REMARKS

This application has been carefully reviewed in light of the Office Action dated May 22, 2006. Claims 2 and 4 to 14 are currently in the application, with Claim 9 being the sole independent claim. Reconsideration and further examination are respectfully requested.

Initially, Applicants thank the Examiner for the indication that Claims 2, 4, 5, 10 and 11 contain allowable subject matter and would be allowable if rewritten in independent form. As discussed below, Applicants believe that all of the claims currently in the application are in condition for allowance. Accordingly, Applicants have not rewritten any of Claims 2, 4, 5, 10 and 11 in independent form at this time.

Claims 4, 9 and 13 were rejected under 35 U.S.C. § 102(b) over U.S. Patent No. 6,444,968 (Burt); Claims 12 and 14 were rejected under 35 U.S.C. § 103(a) over Burt; Claims 6 and 7 were rejected under 35 U.S.C. § 103(a) over Burt in view of U.S. Patent No. 5,214,274 (Yang); and Claim 8 was rejected under 35 U.S.C. § 103(a) over Burt in view of U.S. Patent No. 5,953,110 (Burns). Applicants note that Claim 4 has been rejected under § 102(b) and indicated as containing allowable subject matter in the Office Action. Clarification in the next communication is respectfully requested. With respect to the other rejected claims, Applicants have reviewed the applied references and respectfully submit that the claimed invention is patentably distinguishable over the applied references for at least the following reasons.

Applicants have amended independent Claim 9 to clarify that the photon detector array is bonded to a lateral surface of the stacked configuration of readout electronics integrated circuit chips. In this manner, the photon detector array is arranged perpendicularly to the stacked configuration. This arrangement reduces the overall size of the photon detector module and optimizes the lead lengths between the photo-detectors in the photon detector array and the

channels in the readout electronics integrated circuit chips. This arrangement is neither disclosed nor suggested by the references applied in the Office Action.

Burt is understood to concern a CCD imager that includes an image area (2), a store section (3), an output or read-out register (4), a multiplication register (5) and a charge detection circuit (6). *See* Burt, col. 4, lns. 32 to 37, and Figure 1. The Office Action contended that the image area (2) described in Burt corresponds with the photon detector array of the claimed invention and that the store section (3) described in Burt corresponds with the readout electronics integrated circuit chips of the claimed invention. Even if these correlations were accurate, which Applicants do not concede, Burt is not understood to disclose or suggest the claimed configuration of these components as set forth in Claim 9.

Store section (3) in Burt is depicted in Figure 1 as an array of elements. Nothing in Burt, however, is understood to describe the elements of the store section (3) as being implemented in multiple readout electronics integrated circuit chips. Furthermore, nothing in Burt is understood to describe or suggest that these elements of the store section (3) are arranged in a stacked configuration. At best, Figure 1 of Burt depicts the elements of the store section (3) in a side-by-side array and not a stacked configuration.

The arrangement of the image area (2) with respect to the store section (3) in Burt is also unclear. Figure 1 is not understood to depict the actual arrangement of the CCD imager. Accordingly, reliance on this figure to show a teaching of the claimed arrangement of the invention is improper. Even if Figure 1 were understood to depict the actual arrangement of the CCD imager, the image area (2) is not understood to be bonded to a lateral surface of a stacked configuration of the store section (3) and is definitely not understood to be arranged

perpendicular to the store section (3). Rather, Figure 1 depicts a co-planar arrangement of the image area (2) and the store section (3).

Therefore, Burt is not understood to disclose or even suggest at least the feature of a photon detector array bonded to a lateral surface of a stacked configuration of readout electronics integrated circuit chips such that the photon detector array is perpendicular to the stacked configuration.

The other two references applied against certain dependent claims, namely Yang and Burns, are not understood to disclose or suggest anything to remedy the deficiencies of Burt. Specifically, neither of these references is understood to disclose or suggest at least the feature of a photon detector array bonded to a lateral surface of a stacked configuration of readout electronics integrated circuit chips such that the photon detector array is perpendicular to the stacked configuration.

Therefore, independent Claim 9 is believed to be allowable over the applied references. Reconsideration and withdrawal of the § 102(b) rejection of Claim 9 are respectfully requested.

The other rejected claims in the application are dependent from Claim 9 and therefore are believed to be allowable over the applied references for at least the same reasons. Because each dependent claim is deemed to define an additional aspect of the invention, however, the individual consideration of each is respectfully requested.

In view of the foregoing amendment and remarks, the entire application is believed to be in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience.

Applicants' undersigned attorney may be reached in our Orange County office by telephone at (949) 851-0633. All correspondence should continue to be directed to our address given below.

Respectfully submitted,

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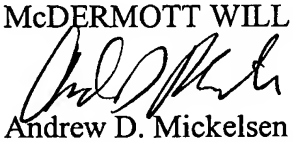

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